PREPARED BY: DATE	SHARP	SPEC NO, LC94Y01
		FILE No.
APPROVED BY: DATE	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	ISSUE NOV. 2,1994
		PAGE 23 Pages
		APPLICABLE DIVISION ■ DUTY PANEL DEVELOPMENT CENTER ❑ ITFT DEVELOPMENT CENTER ❑ ILCD PRODUCTS DEVELOPMENT CENTER ❑ EL PRODUCTION DEPT.
	SPECIFICATION	

DEVICE SPECIFICATION for
Passive Matrix COLOR LCD Unit
(840x480 dots)

Model No,

LM64C21P

❑ ICUSTOMER' S APPROVAL

BY _____

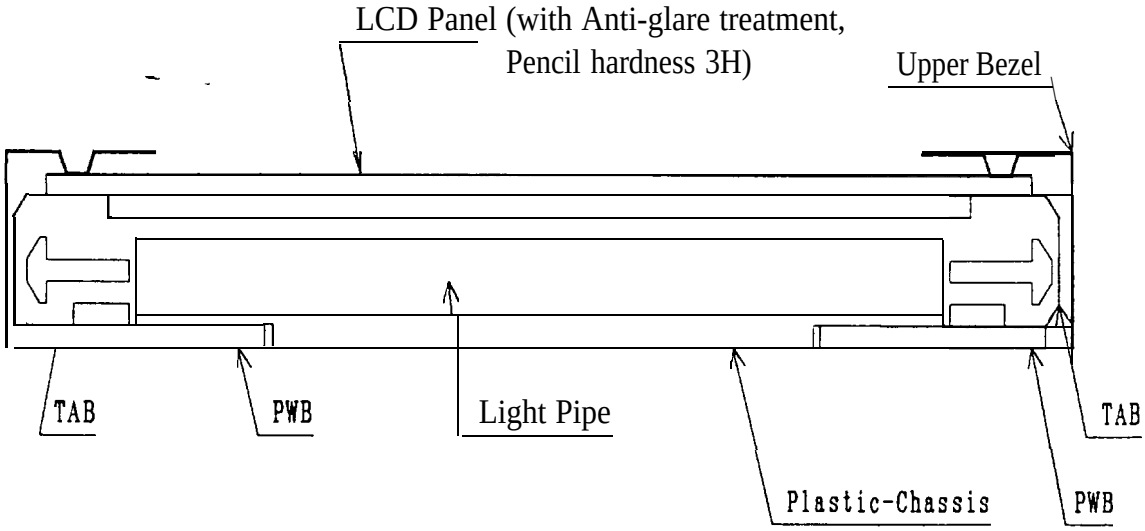
PRESENTED
BY
Y. Inoue
DEPARTMENT GENERAL MANAGER
ENGINEERING DEPARTMENT II
DUTY PANEL DEVELOPMENT CENTER
LIQUID CRYSTAL DISPLAY GROUP
SHARP CORPORATION

1. Application

This data sheet is to introduce the specification of LM64C21P, Passive Matrix type Color LCD Module,

2. Construction and Outline

Construction: 640x480 dots color display module consisting of an LCD panel, PWB (printed wiring board] with electric components mounted onto, TAB (tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically,
Signal ground (VSS) is connected with the metal bezel,
DC/DC converter is built in,



Outline : See Fig, 10
Connection : **See Fig, 10** and Table 6

3, Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	216,0(W) x152.4 (HI×8.0 MAX(D)	mm
Active area	163, 175(W) x122,375(H)	mm
Viewing area	168.8 (W) x 128 (H)	
Display format	640 (W] x480 (H] full dots	-
Dot size	0.085x RGB(W)×0.255 (H)	mm
Dot spacing	0.025	mm
※1 Base color	Normally black ※2	—
Weight	Approx. 280	g

※1 Due to the characteristics of the LC material, the colors vary with environmental temperature,

※2 Negative-type display
Display data "H' : ON → transmission
Display data ' L' : OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 ℃
Input voltage	V_{IN}	-0.3	V_{DD}	V	Ta=25 "C

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 "c	+80 "c	o ℃	+40 "c	Note 4]
Humidity	Note 1]		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z]
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40℃.....95%RH Max

Ta>40 "C... . . Absolute humidity shall be less than Ta=40 "C/95 %RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz 500 Hz
Vibration level	-	9.8 m/s²
Vibration width	0.075 mm	–
Interval	10 Hz～500 Hz～10 Hz/11,0 min	

2 hours for each direction of X/Y/Z (8 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification,

5. Electrical Specifications

5-1 Electrical characteristics

Table 5 $Ta=25\,^{\circ}C$, $V_{DD}=5.0\,V \pm 0.5\,V$

Parameter	Symbol	Conditions	Min.	Typ.	Max,	Unit
Supply voltage (Logic)	$V_{DD}-V_{SS}$	Note 1)	4.5	5.0	5.5	V
Contrast adjust voltage	Vcon -Vss	Ta=O "C	0.80	–	–	V
		Ta=25 "C!	1,35	1.95	2.55	V
		Ta=40 "C			2.80	
Input signal voltage	V_{IN}	'H' level	0.8VDD	–	VDD+0.3	V
		'L' level	0	–	0.2VDD	V
Input leakage current	I_{IL}	'H' level			100	μA
		'L* level	-1oo	–	–	μA
Supply current (Logic)	I_{DD}	Note 2)	–	110	170	mA
Rush current (Logic)	Irush	Ta=25 °C, Power ON	2 A(pk) x20 ms+1 A(pk) x10 μs max			
Power consumption	Pd	Note 2]	–	500	850	mW

Note 1 Under the following conditions, ;

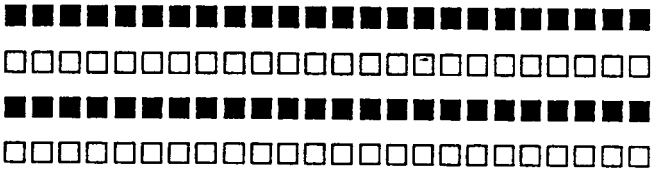
①Immediately after the rise of DISP signal, : 2 Ax20 ms

②Under the situation that DISP signal is on and kept steady. : 1 Ax1O μs

Note 2) Under the following conditions, ;

Vcon-Vss : contrast max. (1.95 V TYP)

V_{DD}-Vss=5.0 V, Frame frequency=73 Hz, Display pattern = black/white stripe pattern



This value is direct current,

5-3 Interface signals

OLCD

Table 6

Pin No	Symbol	Description	Level
1	DL4	Display data signal (Lower)	H (ON), L (OFF)
2	V_{SS}	Ground potential	
3	DL5	Display data signal (Lower]	H (ON), L (OFF)
4	YD	Scan start-up signal	'H'
5	DL6	Display data signal (Lower)	H (ON) , L (OFF)
6	LP	Input data latch signal	'H' → 'L'
7	DL7	Display data signal (Lower)	H (ON) , L (OFF)
8	V_{SS}	Ground potential	–
9	V_{SS}	Ground potential	
10	XCK	Data input clock signal	'H' → 'L'
11	DL0	Display data signal (Lower)	H (ON) , L (OFF)
12	V_{CON}	Contrast adjust voltage	
13	DL1	Display data signal (Lower)	H (ON) , L (OFF)
14	V_{DD}	Power supply for logic and LCD (5. O V)	–
15	V_{SS}	Ground potential	
16	V_{DD}	Power supply for logic and LCD (5. O V)	
17	DL2	Display data signal (Lower)	H (ON) , L (OFFI
18-	DISP	Display control signal	H (ON) , L (OFF)
19	DL3	Display data signal (Lower)	H (ON) , L (OFF)
20	NC		
21	V_{SS}	Ground potential	
22	DU3	Display data signal (Upper)	H (ON) , L (OFF)
23	DU4	Display data signal (Upper)	H (ON) , L (OFF)
24	DU2	Display data signal (Upper)	H (ON) , L (OFF)
25	DU5	Display data signal (Upper)	H (ON) , L (OFF)
26	DU1	Display data signal [Upper]	H (ON) , L (OFF)
27	V_{SS}	Ground potential	–
28	DU0	Display data signal (Upper)	H (ON) , L (OFF)
29	DU6	Display data signal (Upper)	H (ON) , L (OFF)
30	V_{SS}	Ground potential	–
31	DU7	Display data signal (Upper)	H (ON) , L (OFF)

○CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage lineal (from Inverter)	
2	NC		–
3	GND	Ground line (from Inverter)	

NOTE) Pin No, and its location are shown in Fig, 10,

OLCD

Used connector: DF9B-31P-1V (HIROSE)

Mating connector: DF9B-31S-1V (HIROSE)

○CCFT

Used connector: BHR-03VS-1 (JST)

Mating connector: SM03 (4, O) B-BHS or SM02 (8. O) B-BHS (JST)

Except above connector shall be out of guaranty

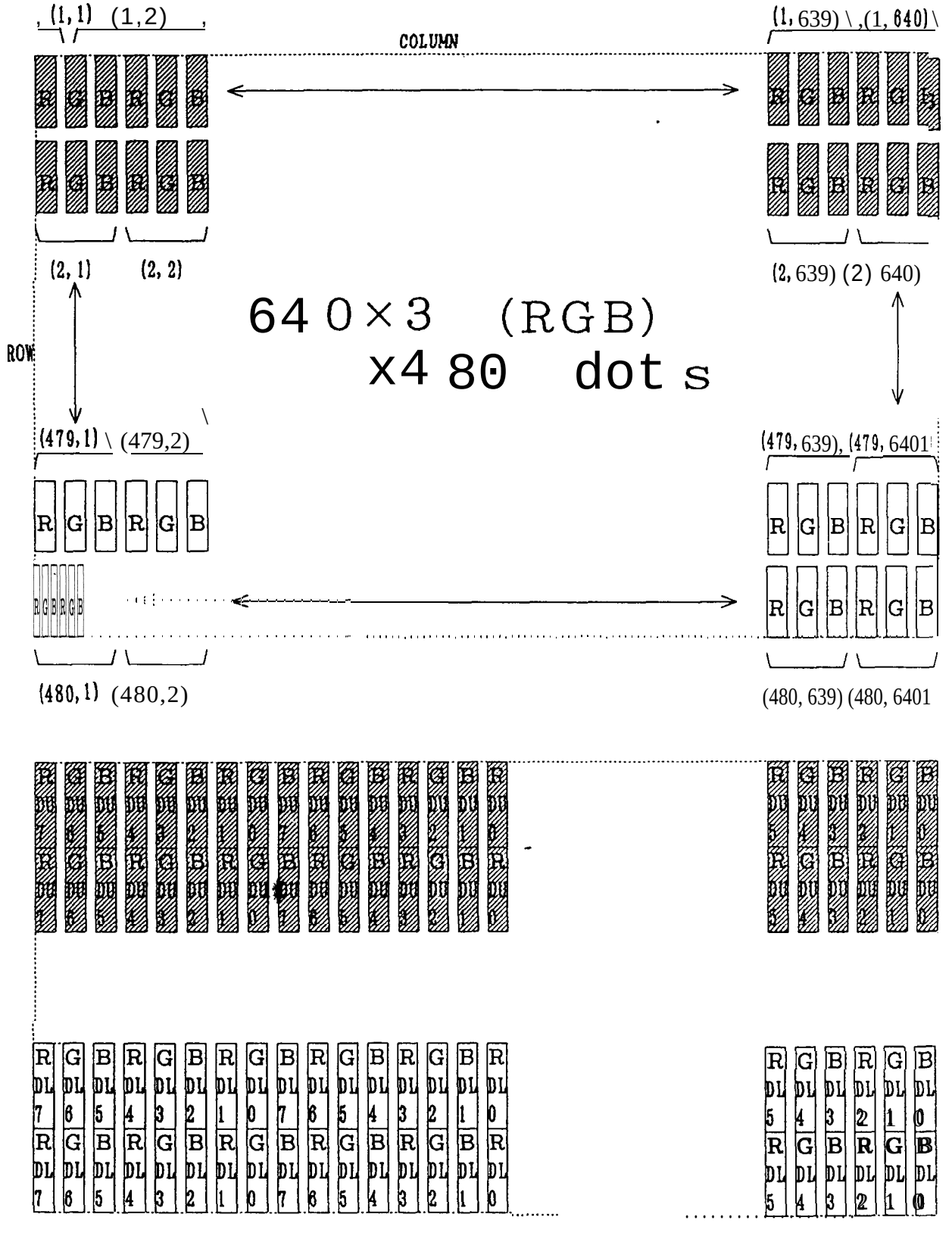
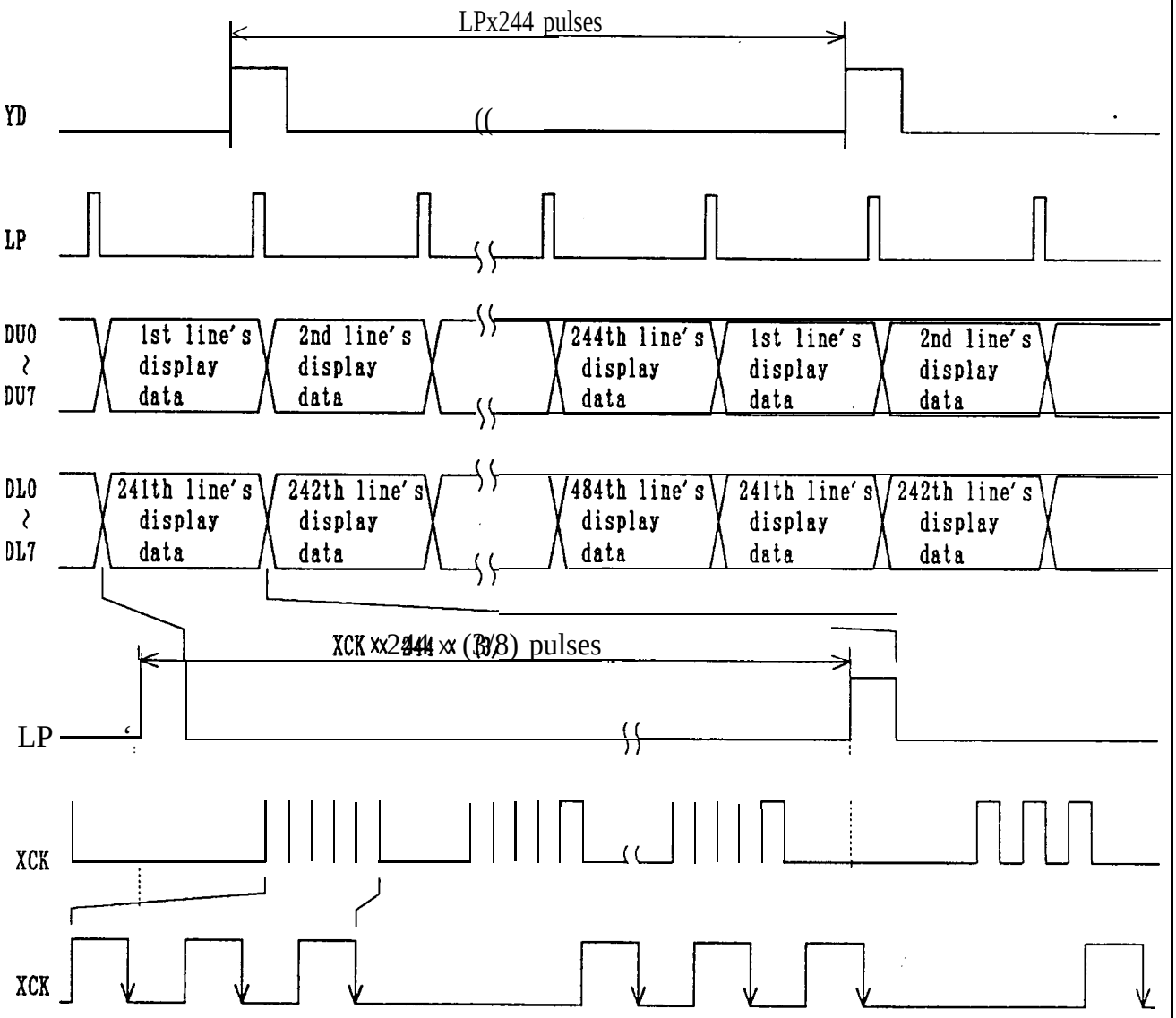


Fig. 1 Dot chart of display area



DU7	R (1, 1)	B (1,31	G (1,6)		R (1, 9)	B(1, 11)	G(I, 14]	
DU6	G (1, I)	R (1, 4)	B (1, 6)		G (1, 9)	R(1) 12)	B(l) 14)	
DU5	E(1, 1)	G (1, 4)	R (1, 7)		B (1, 9)	G(l) 12)	R(l) 15)	
DU4	R (1, 2)	B (1, 4)	G (1, 7)		R(1> 10)	B(1, 12)	G(1, 15)	
DU3	G (1, 2)	R (1,5)	B (1, 7)		G(1, 10)	R(1, 13)	B(1, 15)	
DU2	B (1, 2)	G (1, 5)	R (1, 8)		B(l) 10)	G(I, 13)	R(1, 16)	
DU1	R (1, 3)	B (1, 5)	G (1,8)		R(1, 11)	B(l) 13)	G(l) 16)	
DU0	G (1, 3)	R (1, 6)	B (1, 8)		G (1, 11)	R(1, 14)	B(1, 16)	

DL7	R (241, 1)	B (241,3)	G (241, 6)		R (241, 9)	B (241, 11)	G (241, 14)	
DL6	G (241, 1)	R (241, 4)	B (241, 6)		G (241, 9)	R (241, 12)	B (241, 14)	
DL5	B (241, 1)	G (241,4)	R (241, 7)		B (241, 9)	G (241, 12)	R (241, 15)	
DL4	R (241, 2)	B (241, 4)	G (241, 7)		R (241, 10)	B (241, 12)	G (241, 15)	
DL3	G (241, 2)	R (241, 5)	B (241, 7)		G (241, 101	R (241, 13)	B (241, 15)	
DL2	B (241, 2)	G (241, 5)	R (241, 8)		B (241, 10)	G (241, 13)	R (241, 16)	
DL1	R (241, 3)	B (241, 5)	G (241, 8)		R (241, 11)	B (241, 13)	G (241, 16)	
DL0	G (241, 3)	R (241, 6)	B (241, 8)		G (241, 11)	R (241, 14)	B (241, 16)	

Fig. 2 Data input timing chart

Table. 7 Interface timing ratings (Ta=0～40 "C, VDD=5. O V ±0. 5 V)

Item	Symbol	Rating MIN.	TYP.	MAX,	Unit
Frame cycle *1	tFRM	7. 69		16. 94	ms
YD signal *H' level set up time	tHYS	100			ns
H level hold time	tHYH	100			ns
'L* level set up time	tLYS	100			ns
*L" level hold time	tLYH	40			ns
LP signal * H' level pulse width	tWLPH	200			ns
LP signal clock cycle *3	tLP	10		70	us
XCK signal clock cycle	tCK	70			ns
*H" level clock width	tWCKH	25			ns
' L' level clock width	tWCKL	25			ns
Data set up time	tDS	25	5		ns
hold time	tDH	25			ns
LP ↑ allowance time from XCK ↓	tLS	200			ns
XCK ↑ allowance time from LP ↓	tLH	200			ns
Input signal rise/fall time	tr, tf			*2	ns

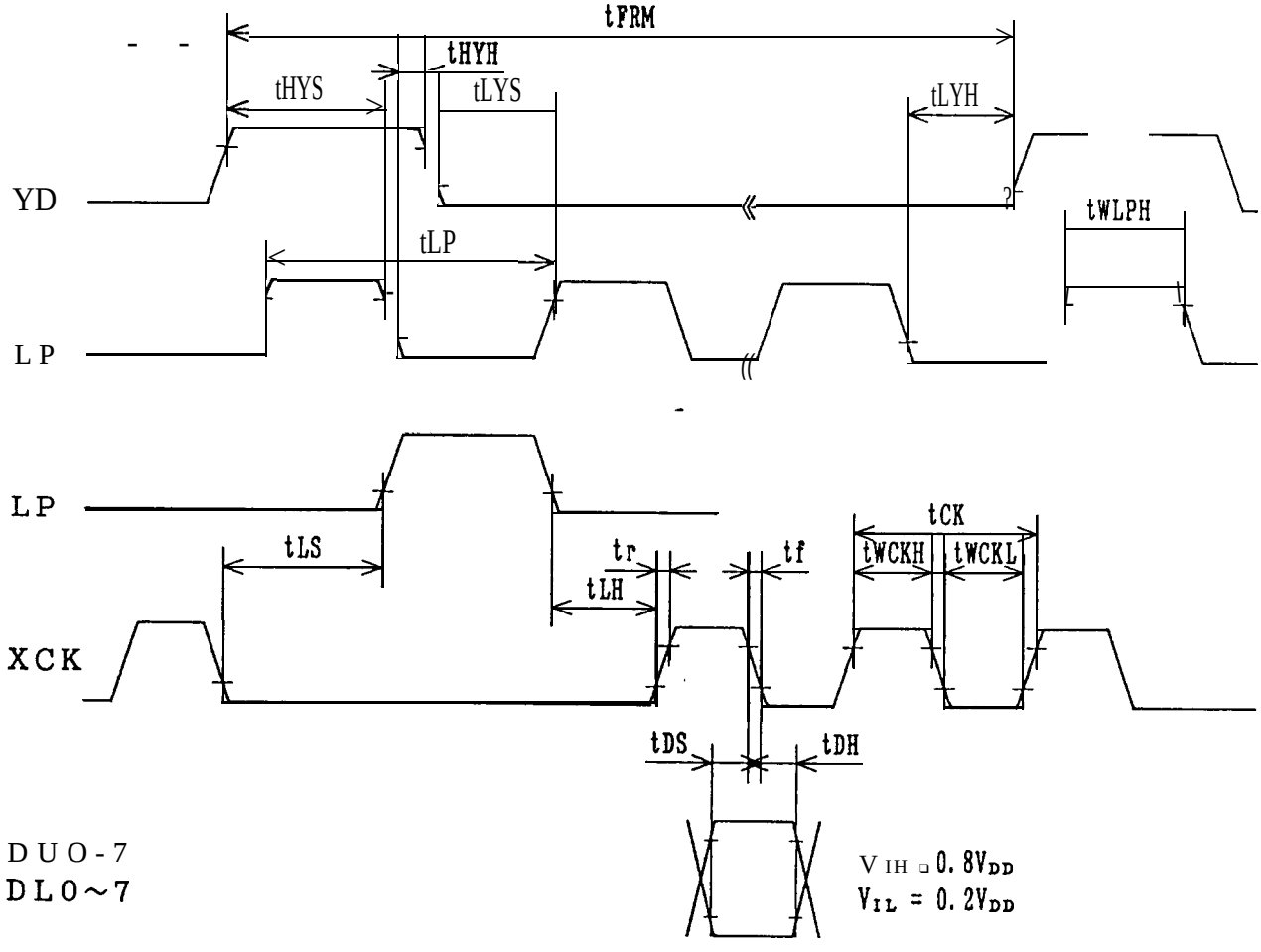


Fig. 3 Interface timing chart

1 LCD unit functions at the minimum frme cycle of 7.69 ms (Maximum frame frequency of 130 HZ)
Owing to the characteristics of LCD unit, * shadowing' will become more eminent as frame frequency goes UP, whle flicker will be reduced,

According to our experiments, frame cycle of 12,8 ms Min. or frame frequency of 78 Hz Max, will demonstrate optimum display quality in terms of flicker and ' shadowing". But since judgement of display quality is subjective and display quality such as 'shadowing' is patturn dependent, it is recommended that decision of frame frequency, to which power consumption of the LCD unit is promotional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it,

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2 \geqq 20$ ns • " " 20 ns MAX
$(t_{CK}-t_{WCKH}-t_{WCKL})/2 < 20$ ns " ." $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ MAX

*3 The intervals of 1 LP fall and the next must be always the same when the LCD UNIT is active driving,
And LP's must be input continuously.

6. Module Driving Method

6.1 Circuit configuration

Fig. 9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 640x3 (R, G, B) x480 dots as shown in Fig, 1.
The interface is single panel with double drive to be driven at 1/244 duty ratio,

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits, Input data for each row (640x3 R, G, B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (640 x 3, R, G, B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge-of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits,

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered, When data for 640x3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row,

Such data : nput will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method,

Simultaneously the same scanning sequence occur at the lower panel,
Then data input proceeds to the next display frame,

YD generates scan signal to drive horizontal electrodes,