AN.No.G649D-331E

LIQUID CRYSTAL DISPLAY MODULE

G649D

USER'S MANUAL

Seiko Instruments Inc.

NOTICE

This manual describes the technical information, as well as the functions and operation of the G649D Liquid Crystal Display Module made by Seiko Instruments Inc. Please read this manual carefully to familiarize yourself with the functions so you can make the best use of them.
The descriptions here are subject to change without notice.

Revision Record

Edition	Revision	Date
1	Original	June 1992
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1. SPECIFICATIONS

1.1 General

The G649D is a thin liquid crystal display (LCD) module that consists of a full dot-matrix LCD panel, CMOS LSIs, and a CFL backlight. The LCD panel features a wide viewing angle and high contrast. The full dot-matrix structure allows both graphics and character display. In addition, the display is clear and stable, with no image warping or position skew, because the display position is specified by the intersection of transparent electrodes in a matrix.

1.2 Features

- Full dot-matrix structure with 640 × 200 dots
- 1/200 duty cycle
- Four-bit parallel data input
- Two power supplies : V_{DD} = 5 V, V_{LC} = -24 V (for driving liquid crystal)
- Built-in CFL backlighting, high-brightness, side-lighting type, using one CFL
- Weight : Approx. 420 g

1.3 Option Specifications

Model name	LCD	Dot color*	Background color*	Viewing angle	
G649DX5R010	FSTN type (black and white)	White	Black	6 o'clock	Transmissive, with CFL backlighting (white), negative type**
G649DX5B010	STN type (blue)	White	Blue	6 o'clock	Transmissive, with CFL backlighting (white), negative type**

* The LCD colors are affected by temperature, so the colors at low or high temperature differ slightly from those in the above table.

** On a negative type LCD, the dots are white when the display data is high, and black (G649DX5R010) or blue (G649DX5B010) when the display data is low. To get a positive display on a negative type LCD, invert the display data before inputting it to the module.

1.4 Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply voltage	V_{DD}		0	6.0	V
	V_{LC}		V_{DD} – 30.0	V_{DD}	V
	V_O	$V_O \geqq V_{LC}$	V_{DD} – 30.0	V_{DD}	V
Input voltage	V_{IN}		– 0.3	V_{DD} + 0.3	V
Operating temperature	T_{opr}		0	+ 50	°C
Storage temperature	T_{stg}		– 20	+ 60	°C

1.5 Electrical Characteristics (Excluding CFL Backlight)

1.5.1 FSTN type (Black and white, transmissive type)

Vss = 0 V, Ta = 0°C to 50°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V ± 5%	− 24.5	− 24.0	− 23.5	V
		V_O	V_{DD} = 5 V ± 5%, $V_O \geqq V_{LC}$	− 23.0	—	—	V
Input voltage	High	V_{IH}	V_{DD} = 5 V ± 5%	0.8 V_{DD}	—	V_{DD}	V
	Low	V_{IL}	V_{DD} = 5 V ± 5%	0	—	0.2 V_{DD}	V
Current consumption		I_{DD}	V_{DD} = 5.0 V, V_{LC} = − 24.0 V, V_O = − 17.0 V	—	11	25	mA
		I_{LC}		—	9	20	mA
Frame frequency		f_{FRM}	V_{DD} = 5 V ± 5%	65	70	75	Hz

1.5.2 STN type (Blue, transmissive type)

Vss = 0 V, Ta = 0°C to 50°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V ± 5%	− 24.5	− 24.0	− 23.5	V
		V_O	V_{DD} = 5 V ± 5%, $V_O \geqq V_{LC}$	− 23.0	—	—	V
Input voltage	High	V_{IH}	V_{DD} = 5 V ± 5%	0.8 V_{DD}	—	V_{DD}	V
	Low	V_{IL}	V_{DD} = 5 V ± 5%	0	—	0.2 V_{DD}	V
Current consumption		I_{DD}	V_{DD} = 5.0 V, V_{LC} = − 24.0 V, V_O = − 16.3 V	—	11	25	mA
		I_{LC}		—	9	20	mA
Frame frequency		f_{FRM}	V_{DD} = 5 V ± 5%	65	70	75	Hz

1.6 Optical Characteristics

1.6.1 FSTN type (Black and white, transmissive type)

1 / 200 duty, 1 / 15 bias, V_{opr} = 22.0 V, Ta = 25°C

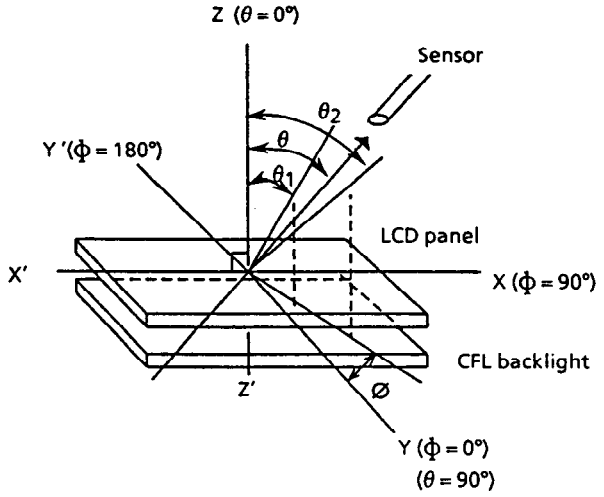
Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	C ≧ 2.0, ϕ = 0°	55°	–	–	Notes 1 & 2
Contrast	C	θ = − 10°, ϕ = 0°	5	8	–	Note 3
Response time (rise)	t_{on}	θ = 0°, ϕ = 0°	–	250 ms	380 ms	Note 4
Response time (fall)	t_{off}	θ = 0°, ϕ = 0°	–	150 ms	150 ms	Note 4

1.6.2 STN type (Blue, transmissive type)

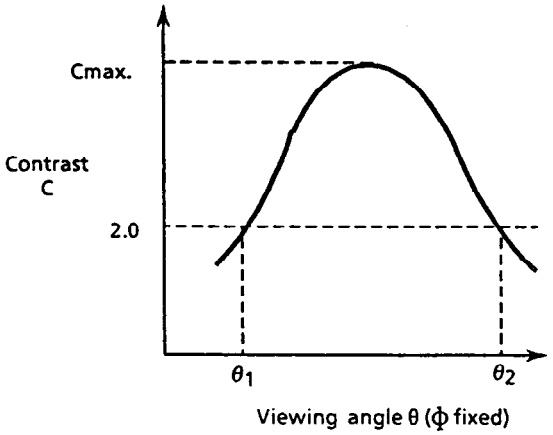
1 / 200 duty, 1 / 15 bias, V_{opr} = 21.3 V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	$C \geqq 2.0$, $\phi = 0°$	35°	–	–	Notes 1 & 2
Contrast	C	$\theta = 5°$, $\phi = 0°$	2	3.5	–	Note 3
Response time (rise)	t_{on}	$\theta = 0°$, $\phi = 0°$	–	250 ms	380 ms	Note 4
Response time (fall)	t_{off}	$\theta = 0°$, $\phi = 0°$	–	150 ms	230 ms	Note 4

Note 1 : Definition of angles θ and ϕ



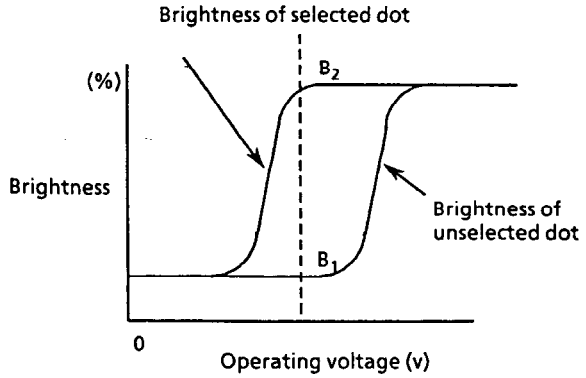
Note 2 : Definition of viewing angles $\theta 1$ and $\theta 2$



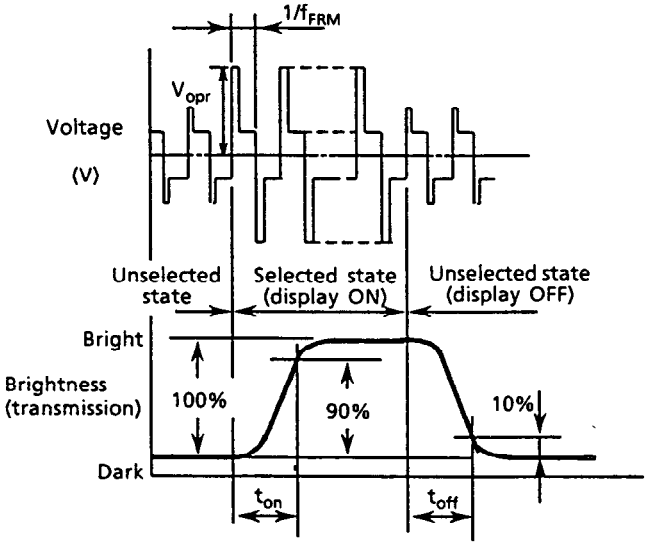
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. above are not always the same.

Note 3 : Definition of contrast C

$$C = \frac{\text{Brightness of selected dot } (B_2)}{\text{Brightness of unselected dot } (B_1)}$$



Note 4 : Definition of response time



V_{opr} : Operating voltage
t_{on} : Response time (rise)
f_{FRM} : Frame frequency
t_{off} : Response time (fall)

1.7 Dimensions

Unit : mm/inch

General tolerance : ± 0.5 mm(0.02inch)

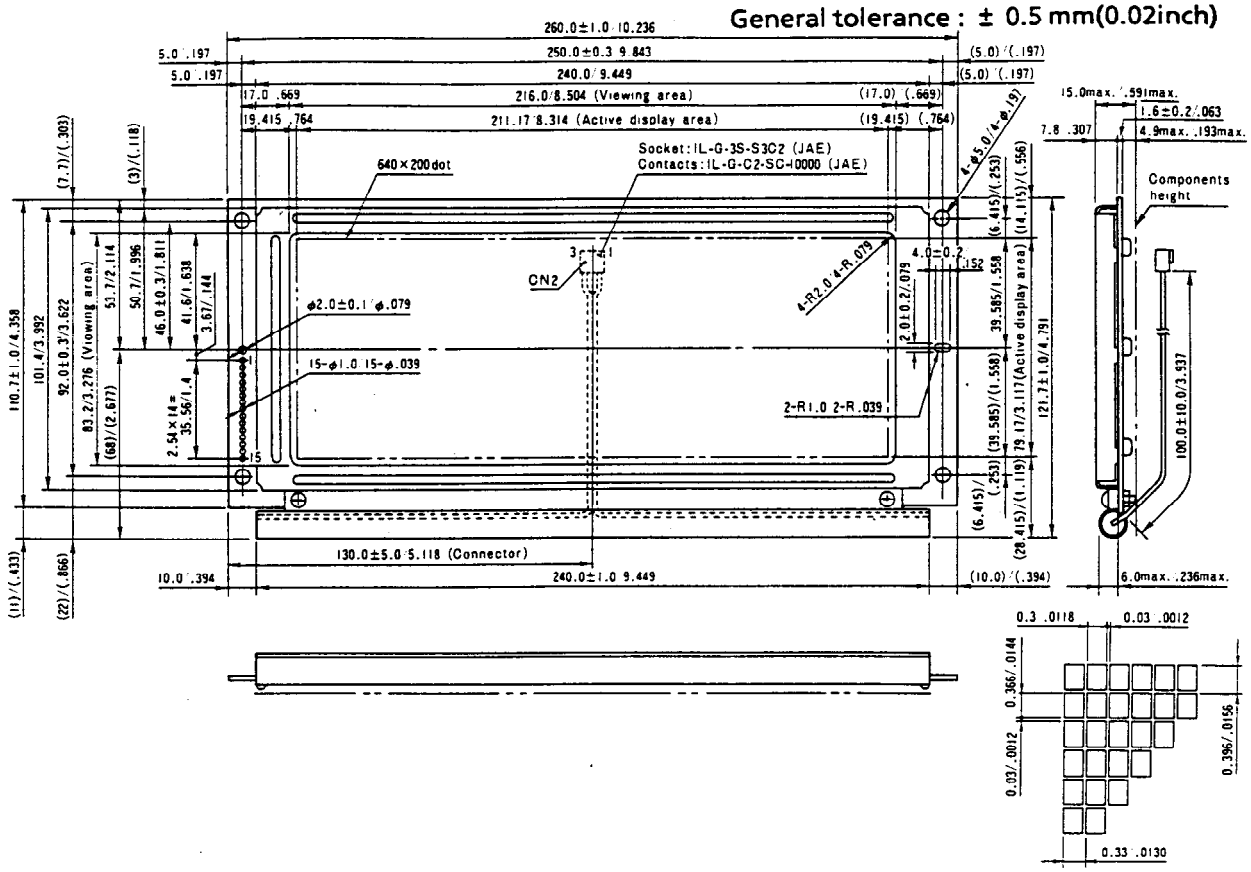


Figure 1 Dimensions

[I/O Terminal Functions]

CN1

No.	Symbol	Function
1	V_{DD}	Power supply voltage (1) : + 5 V
2	F_{GND}	Frame ground*
3	CL2	Display data shift clock
4	INH	Display ON/OFF control terminal**
5	FLM	One-frame timing signal
6	CL1	One-common-line timing signal
7	V_{SS}	GND : 0 V
8	M	NC (or liquid crystal AC drive control signal)

No.	Symbol	Function
9	D_0	Display data input
10	D_1	Display data input
11	D_2	Display data input
12	D_3	Display data input
13	V_{LC}	Power supply voltage (2) : – 24 V
14	V_O	Liquid crystal drive voltage adjustment terminal
15	V_{SS}	GND : 0 V

* The F_{GND} terminal is connected to the module metal frame. Use this terminal to ground the frame.

** The display is on when INH is H, and off when L.

CN2

CFL connector: socket IL-G-3S-S3C2 (JAE), socket contact IL-G-C2-SC-10000 (JAE)

Mating connector (board mount type): IP-G-3P-S3T2-E (straight type) (JAE)

IL-G-3P-S3L2-E (right-angle type) (JAE)

No.	Symbol	Wire color	Function
1	V_{FLG}	White	GND*: 0 V
2	NC	—	NC
3	V_{FL1}	White	CFL backlight drive signal

* Not connected to V_{SS} (GND) of CN1.

2. CIRCUIT STRUCTURE

2.1 Liquid Crystal Driving Circuit

The G649D LCD panel drive waveform is shown in Figure 2. Since DC voltage will damage the liquid crystal, AC voltage is applied between the two frames. The signal controlling this is the liquid crystal AC drive control signal *M*.

Depending on the LCD panels, increasing the liquid crystal AC drive waveform frequency may improve the display quality. The G649D contains a circuit that generates AC drive control signal *M'*, which has a higher frequency than that of *M*. The frequency of the *M'* signal is adjusted according to the LCD panel to provide the best display quality. The use of an external *M* signal is also possible if necessary.

The liquid crystal driving circuit using an *M'* signal does not require an *M* signal to be input. However, the interface circuit should be provided with *M* signal input for compatibility with the liquid crystal driving circuit using a *M* signal.

The frame frequency is normally set to 70±5 Hz to prevent screen flicker.

The G649D has a 1/200 duty cycle, and the common electrodes are selected within a frame by time division from electrode 1 to electrode 200. This is called line sequential scanning. The voltage level of the segment electrodes determines whether or not the dots at the intersection of the segment electrodes are selected when the common electrode is selected. As shown in Table 1, there are six drive waveform voltage levels, V_a to V_f. The voltage level is determined by the bias value. The voltage between the segment and common electrodes is then applied to the liquid crystal. The selection waveform for SEG_0-COM_0 and the non-selection waveform for SEG_1-COM_1 are shown in Figure 2. The size of the effective voltage of the waveform determines whether the liquid crystal under the selected dots is in the selection or non-selection state.

Table 1

V_a	Common and segment selection level
V_b	Common non-selection level
V_c	Segment non-selection level
V_d	Segment non-selection level
V_e	Common non-selection level
V_f	Common and segment selection level

In black-and-white negative mode, the dot is white when the display data is "1" and black when "0". In blue negative mode, the dot is white when the display data is "1" and blue when "0".

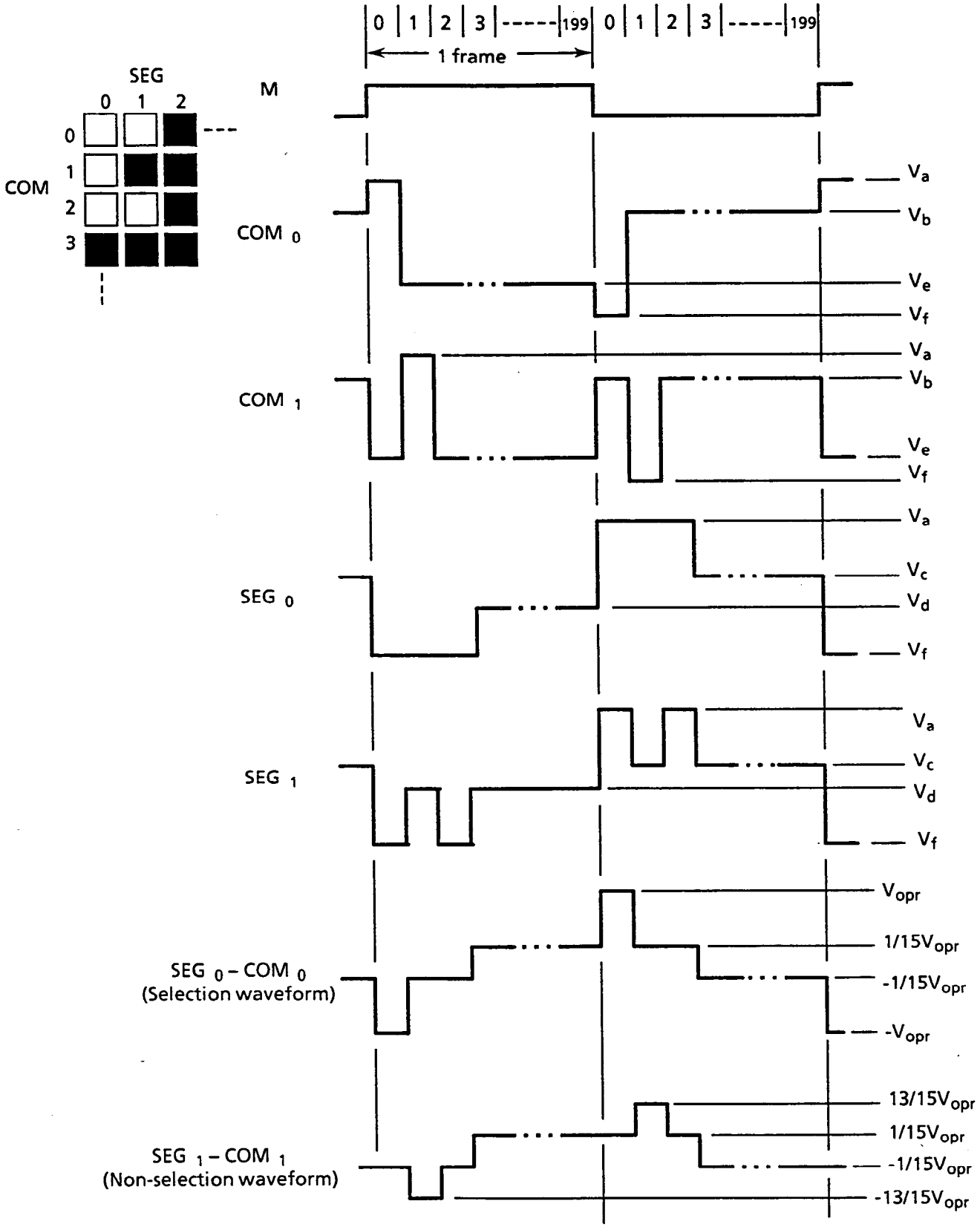


Figure 2 Drive Waveform

2.2 Circuit Structure

The G649D consists of common drivers, segment drivers, a bias voltage generation circuit, an *M'* generation circuit and a V_{opr} control circuit. Figure 3 shows the block diagram for the G649D. When an *M* signal is used instead of an *M'* signal, the *M* signal is directly input to the segment drivers and the common drivers.

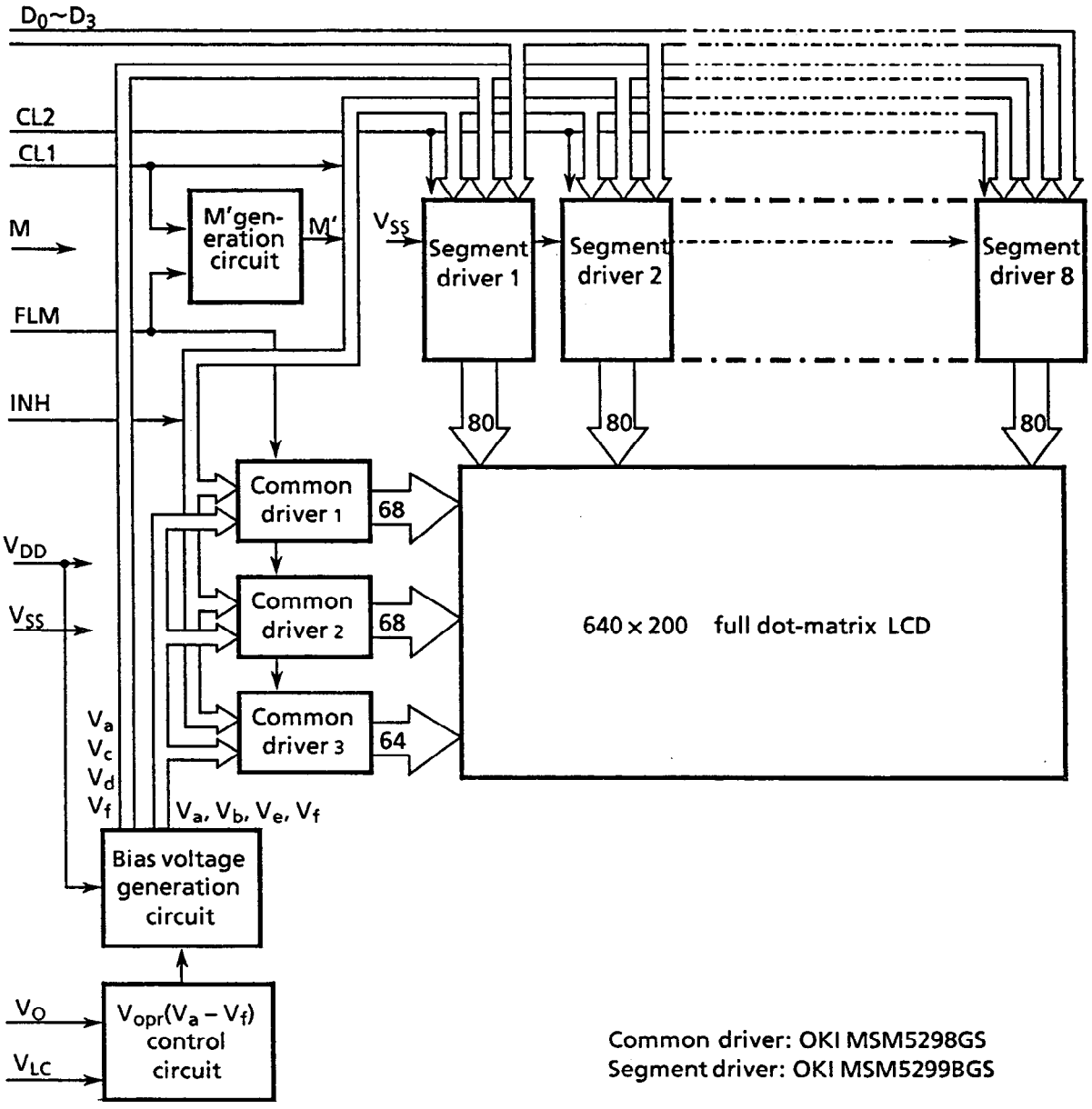


Figure 3 Block Diagram for G649D

(1) Common driver (OKI MSM5298GS)

A common driver (CD) is a CMOS IC with 68 drive outputs. The G649D has three CDs, whose internal registers are connected to each other. They operate as follows.

Input one-frame timing signal (FLM) is taken into the internal shift register by the falling edge trigger of the one-common-line timing signal (CL1), and sequentially shifted. After 200-CL1 input, the next FLM is input and the same operation is repeated. As shown in Table 2, the common output is selected according to the shift register contents and the internally-generated liquid crystal AC drive control signal (M') in the drive circuit, and the common drive waveform are formed.

Table 2

INH	Shift register content	M'	COM output
H	H	H	V_a
		L	V_f
	L	H	V_e
		L	V_b
L	×	×	V_a

×: Invalid

The common output is controlled by the INH signal; when the INH signal is low, the common output is V_a, irrespective of the shift register contents or the M' signal.

(2) Segment driver (OKI MSM5299BGS)

A segment driver (SD) is a CMOS IC with 80 drive outputs. The G649D has eight SDs, which operate as follows.

Input four-bit data is sequentially taken into the internal register by the falling edge trigger of the display data shift clock (CL2). The SDs have a chip enable function. After 80 bits of data are taken into SD1, the next bit of data is automatically taken into SD2. Since G649D has eight SDs, 640 bits of data can be taken. The display data taken into the internal register are latched by the falling edge trigger of CL1. The segment output is selected according to this display data and *M'* in the drive circuit, and the segment drive waveform is formed as shown in the Table 3.

Table 3

INH	Display data	M'	SEG output
H	H	H	V_f
		L	V_a
	L	H	V_d
		L	V_c
L	×	×	V_a

×: Invalid

The segment output is controlled by the INH signal. When the INH signal is low, V_a is output to the segment, irrespective of the display data and of the *M'* signal. Therefore, by bringing the INH signal to low, V_a is output both to the common and to the segment electrodes, making the voltage applied to the liquid crystal zero, and the display goes off.

The relationship between the display data and display screen is shown below..

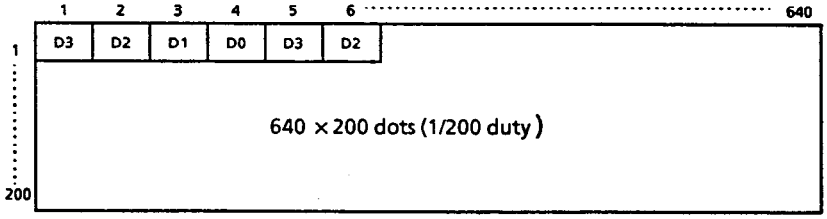


Figure 4

(3) V_{opr} control circuit

Display screen contrast and viewing angle are affected by changes in the liquid crystal operating voltage (V_{opr}). As shown in Figure 5, external V_{LC} is supplied to the operational amplifier and V_{opr} (V_a to V_f) is generated and applied to the LCD panel.

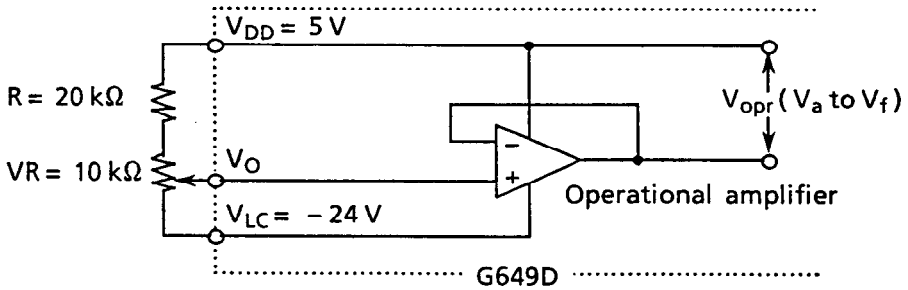


Figure 5

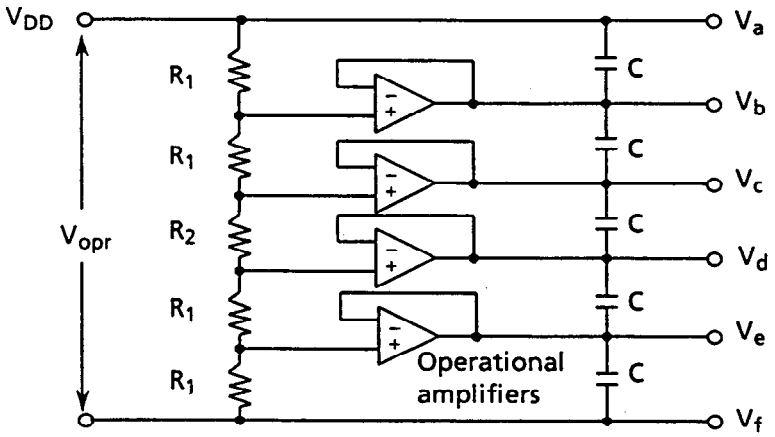
Also, display screen contrast and viewing angle are influenced by the ambient temperature. The recommended V_{opr} level at different temperatures is as follows.

Temperature (°C)		0	25	50
V_{opr} (V)*	FSTN (Black and white)	23.5	22.0	19.5
	STN (Blue)	22.8	21.3	19.4

* $V_{opr} \approx V_{DD} - V_O$

(4) Bias voltage generation circuit

Six voltage levels, V_a to V_f, are applied to the common and segment drivers. The voltage is generated through operational amplifiers by resistance division from the liquid crystal operating voltage (V_{opr}). Here, an operational amplifier is used as a voltage follower.



1 / 15 bias : $R_2 = (15 - 4)R_1 = 11\,R_1$

Figure 6 Bias Voltage Generation Circuit

(5) M' generation circuit

As Figure 7 shows, the M' generation circuit performs an XOR on the one-common-line timing signal (CL1) (on which A time division is performed) and the one-frame timing signal (FLM) (on which B time division is performed), and outputs liquid crystal AC drive control signal M'. Values A and B are set according to the LCD panel so that the best display quality can be obtained and the drive voltage can be changed.

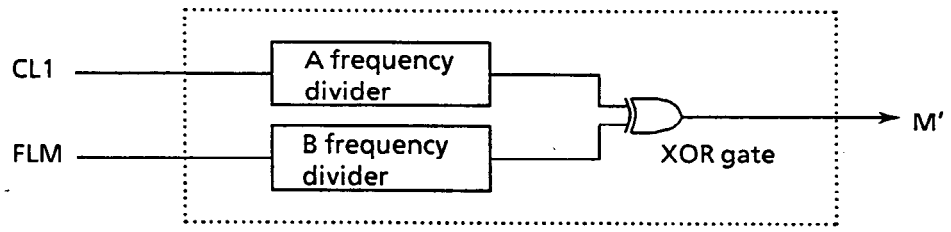


Figure 7 M' Generation Circuit

2.3 Timing Characteristics

2.3.1 Power ON/OFF and Signal Input Timing

Power ON/OFF and signal input should be performed according to the timing shown in the figure below in order not to damage the LCD driving circuit and the LCD panel.

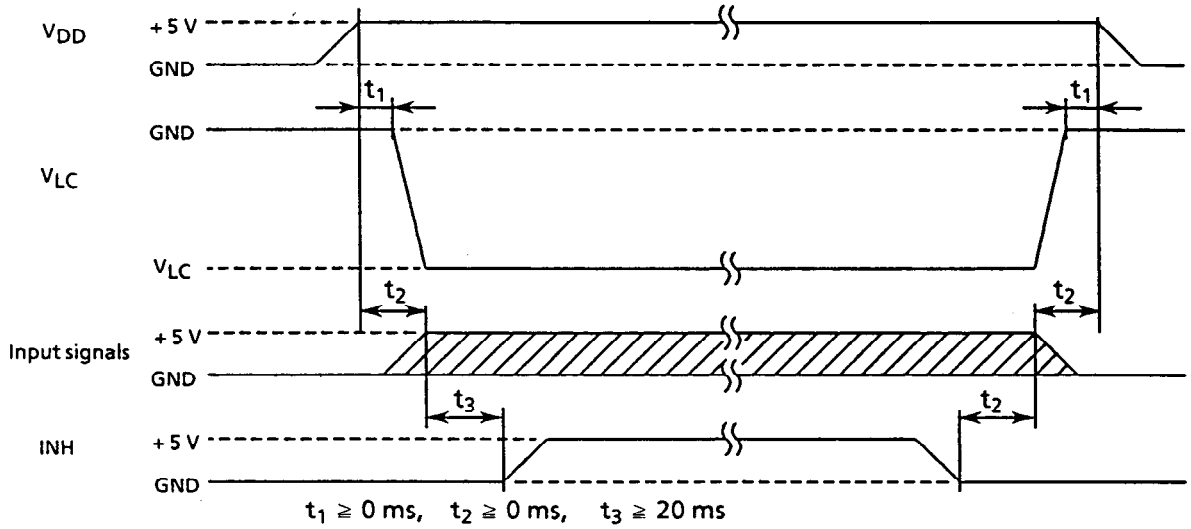


Figure 8 Power ON/OFF and Signal Input Timing

2.3.2 Timing Characteristics

T_a = 0°C to 50°C, V_{DD} = 5.0 V ± 5%

Item	Symbol	Min.	Max.	Unit
CL1 period	tccl1	1000	—	ns
CL1 high pulse width	twcl1h	125	—	ns
CL1 low pulse width	twcl1l	—	—	ns
Data setup time 1	tds1	100	—	ns
Data hold time 1	tdh1	100	—	ns
Allowable M delay time	tdm	—	—	ns
Input signal rise time	t_r	—	50	ns
Input signal fall time	t_f	—	50	ns
CL2 period	tccl2	334	—	ns
CL2 high pulse width	twcl2h	125	—	ns
CL2 low pulse width	twcl2l	125	—	ns
Data setup time 2	tds2	100	—	ns
Data hold time 2	tdh2	100	—	ns
CL2 rise to CL1 rise	tld	63	—	ns
CL2 fall to CL1 fall	tsl	125	—	ns
CL1 rise to CL2 rise	tls	125	—	ns
CL1 fall to CL2 fall	tlh	63	—	ns

Timing Chart 1: Timing of Signal Input Into Common Driver

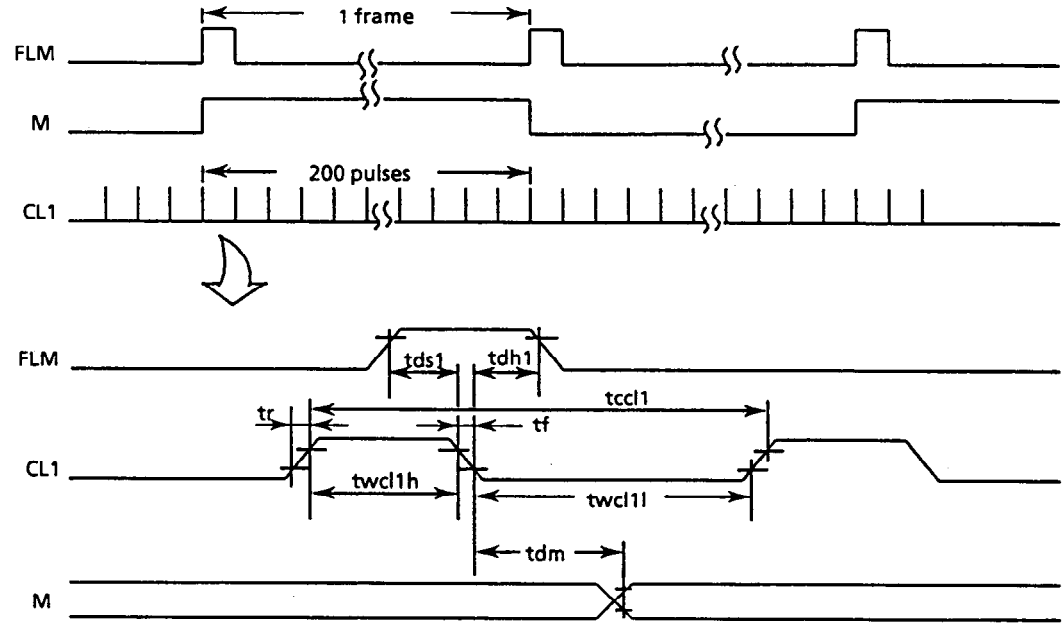


Figure 9

Timing Chart 2: Timing of Signal Input Into Segment Driver

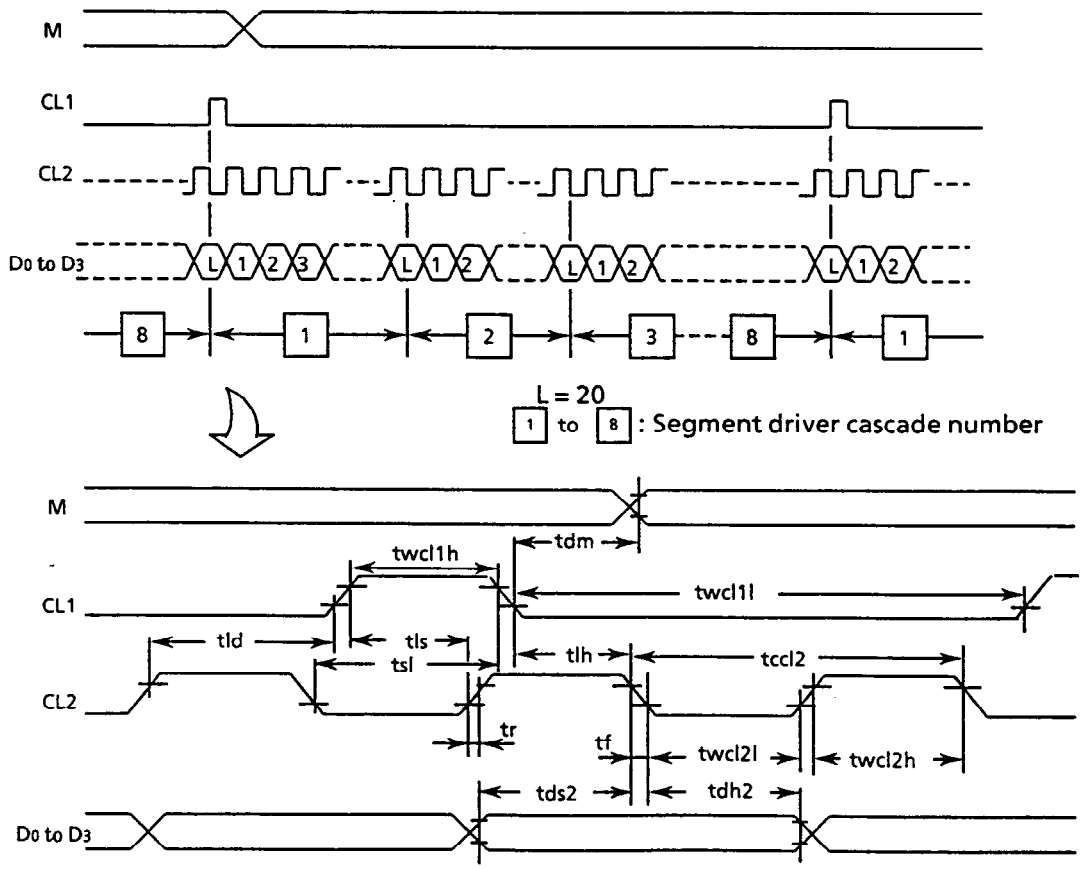


Figure 10

2.4 Interface Circuit

2.4.1 Interface with MPU signal

The G649D is controlled by the MPU circuit, whose interface is easily set up when the LCD controller is used. The LCD controller has basic functions such as receiving information related to the display from the MPU circuit, sending display timing signals and display data to the LCD module, as well as other functions such as cursor display.

The G649D must use an LCD controller conforming to the following:

- For a full dot-matrix LCD module
- Where data is transferred to the LCD module in four-bit parallel
- Where G649D display screen has 1/200 duty

The following section gives examples of interfaces using the Oki MSM6255GSK, Seiko Epson SED1330F, and Hitachi HD64646FS controllers.

(1) OKI MSM6255GSK

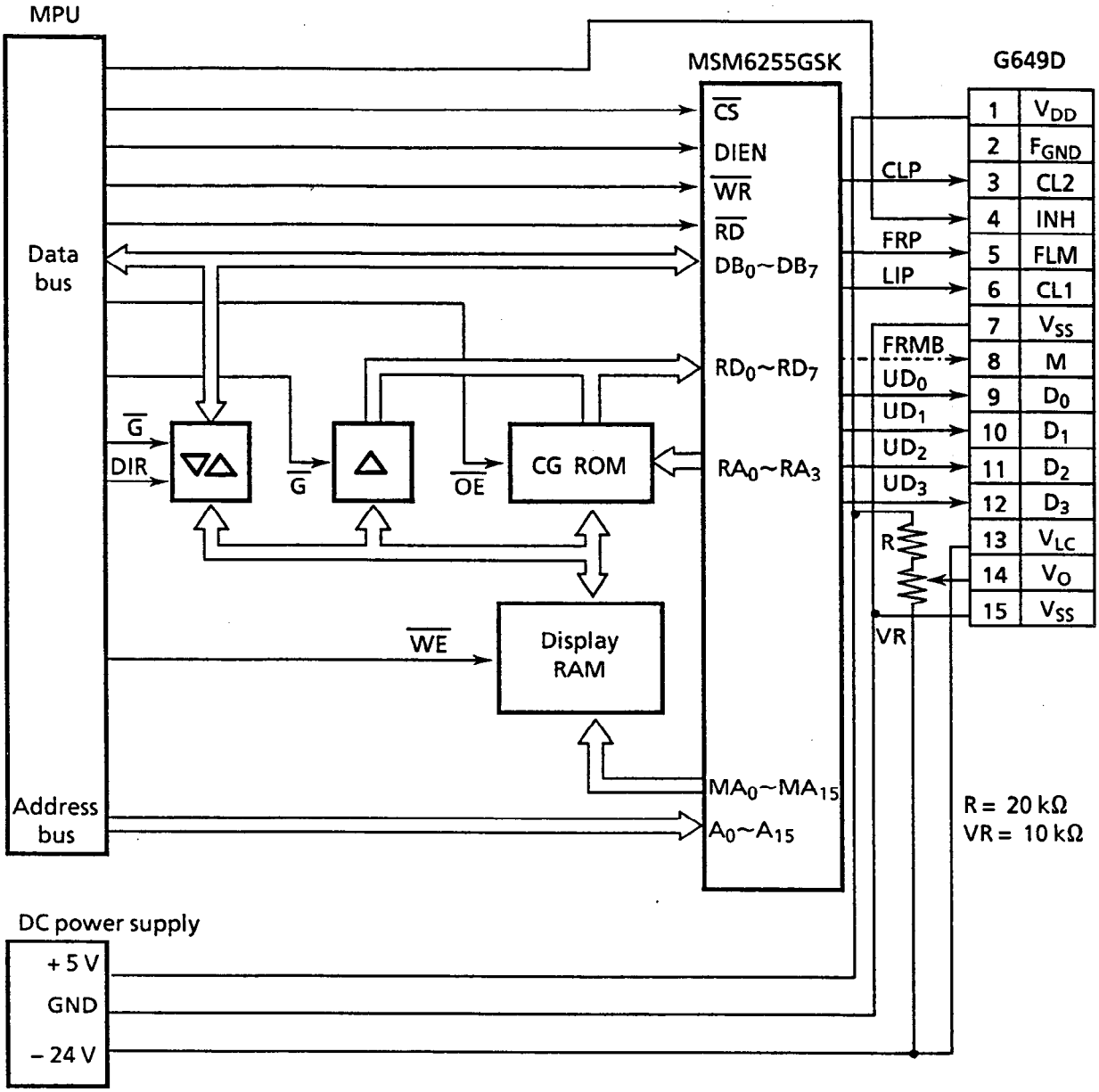


Figure 11 Interface Circuit With MSM6255GSK

Features of the MSM6255GSK:

- Interface with 80-series MPU possible
- Cursor
  - ON/OFF
  - Blinking speed, form, and position are programmable
- Scrolling and paging
- CMOS process
- 5-V single power supply

(2) SEIKO EPSON SED1330F

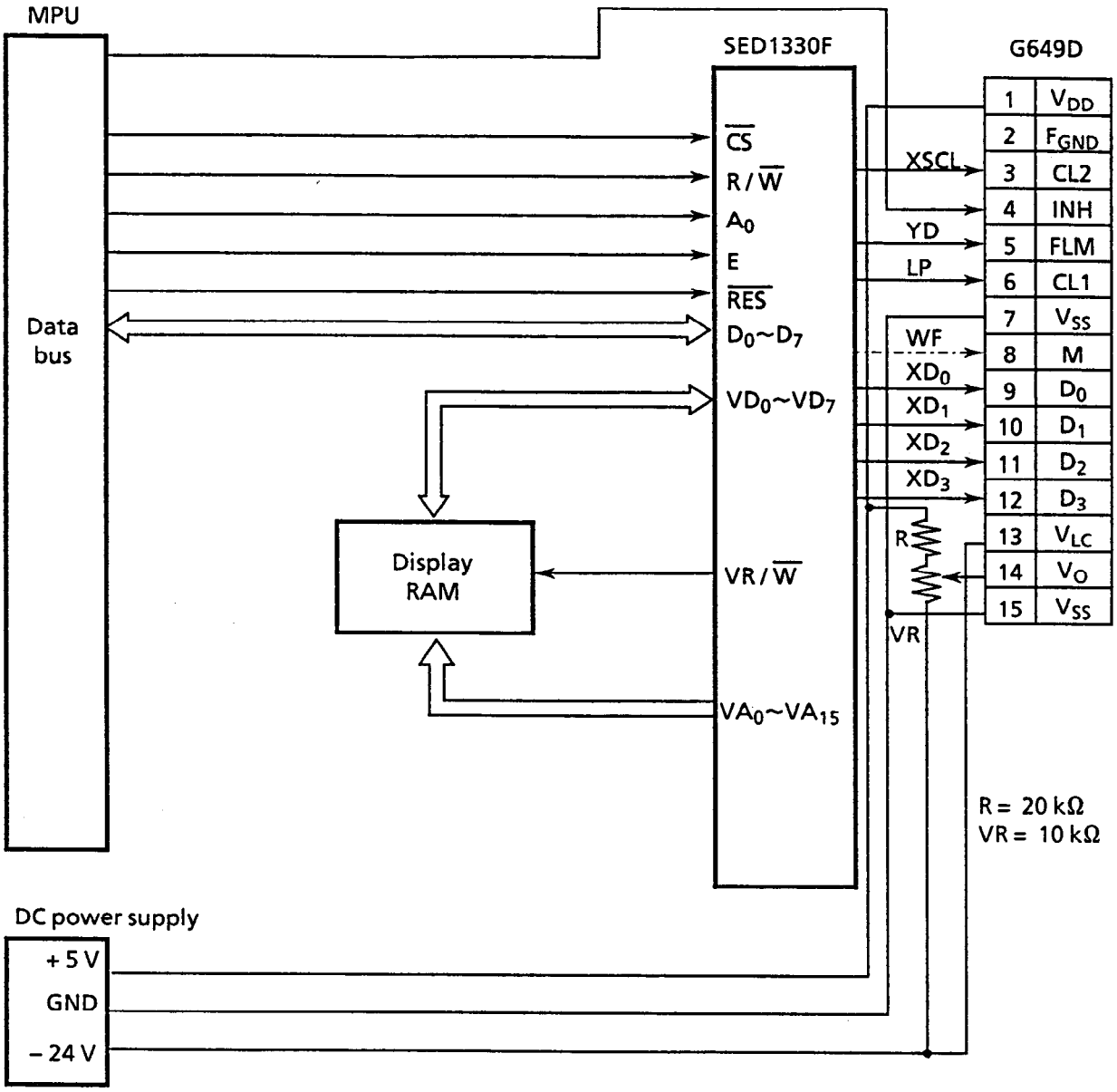


Figure 12 Interface Circuit With SED1330F

Features of the SED1330F:

- Interface with 80-series or 68-series MPU possible
- Built-in character generator ROM: 160 kinds
- External character generator
  - · CG RAM : (8×16 dot matrix)×64 kinds
  - · CG ROM : (8×16 dot matrix)×256 kinds
- Layered mode : AND, OR, XOR, "preferred" OR
- CMOS process
- Scrolling (vertical and horizontal)
- 5-V single power supply

(3) HITACHI HD64646FS

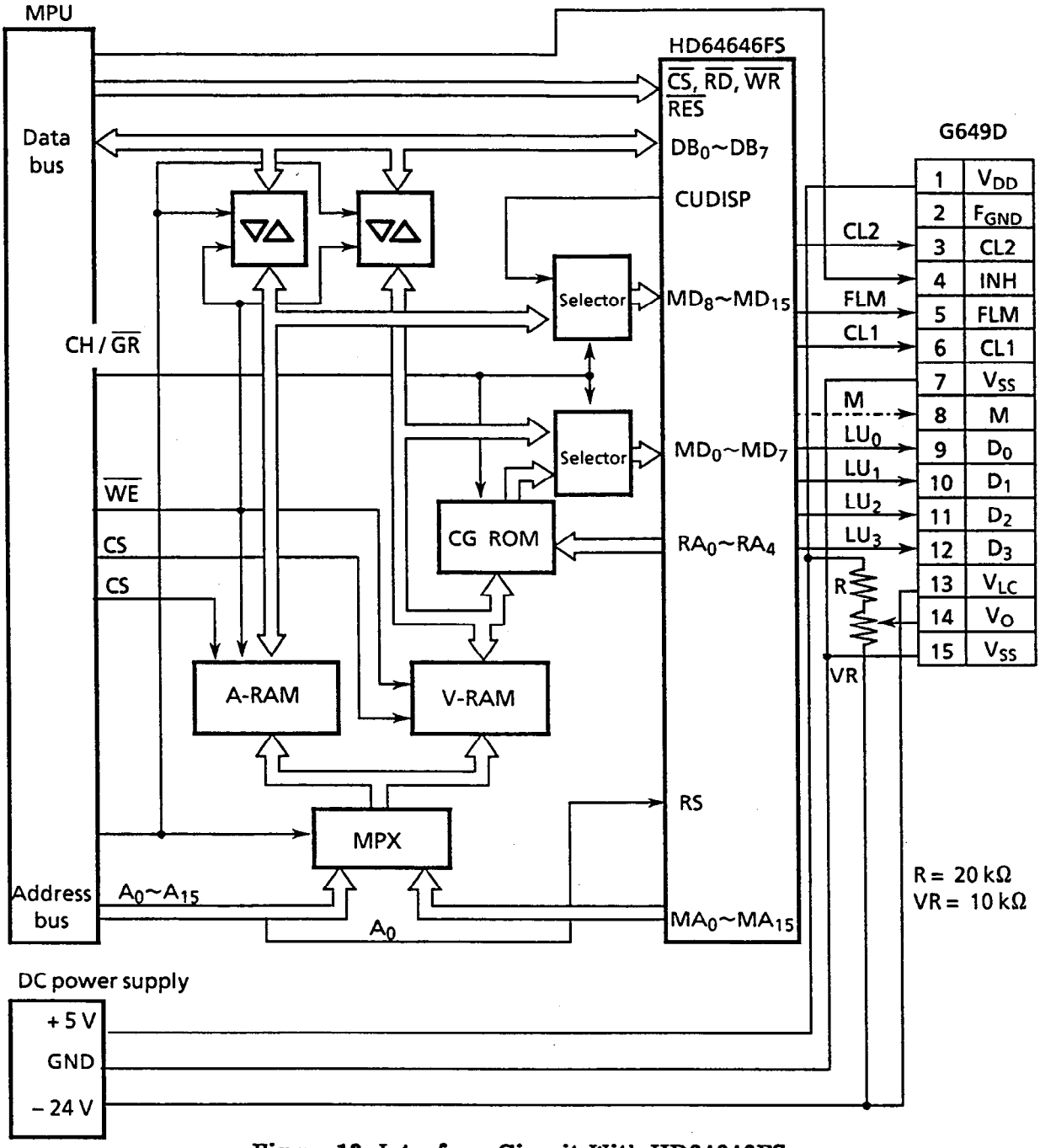


Figure 13 Interface Circuit With HD64646FS

Features of the HD64646FS:

- Interface with 80-series MPU possible
- Layered mode : OR (character and graphics)
- Character reverse, blinking, all black, all white
- Cursor
  - · ON/OFF
  - · Blinking speed, form and position are programmable
- Character font
  - · Vertical : 1 to 32 dots
  - · Horizontal : 8 dots
- Scrolling
  - · Vertical : smooth or character unit
  - · Horizontal : character unit
- CMOS process
- 5-V single power supply

2.4.2 Interface with video signal

When interfacing with SEIKO EPSON SED1341F controller, the G649D can display using separate video signals, without changing hardware or software. Both SED1341FOB and SED1341FOC can be used for G649D interface.

Figure 15 shows an example of interface circuit using the SED1341F.

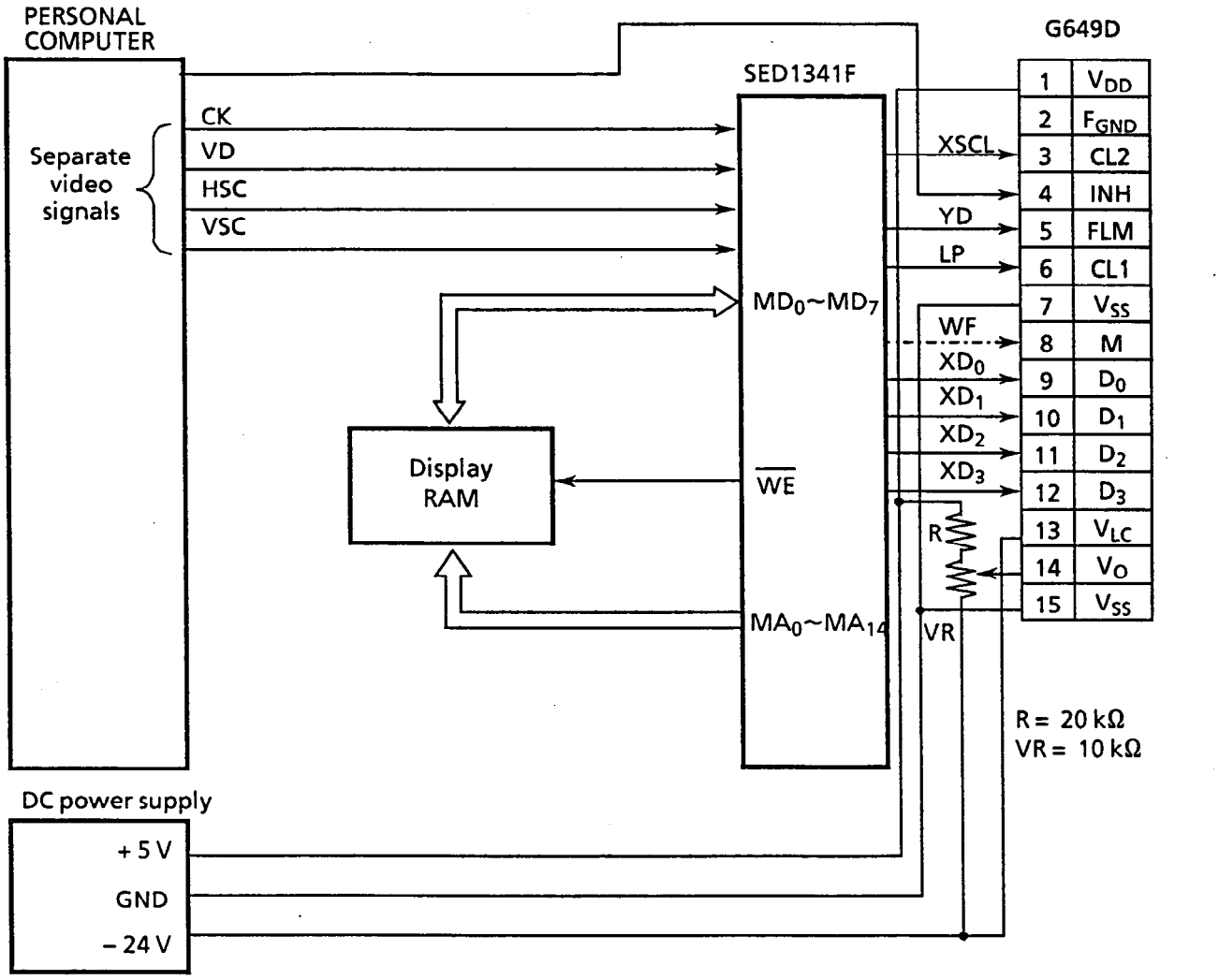


Figure 14 Interface Circuit With SED1341F

Features of the SED1341F:

- Separate signal input compatible with TTL
  - · Video data, Horizontal synchronizing signal, Vertical synchronizing signal, Dot clock
- Dot clock generation with PLL, which has a built-in PLL program counter and phase comparator. Clock frequency is selectable from 14.32 and 21.05 MHz typ.
- Fine adjustment of display position
  - · Register programming method via four-bit bus
- 5-V single power supply

3. CFL BACKLIGHTING

The G649D has a built-in CFL (cold cathode fluorescent lamp) backlight. A CFL inverter is not built in, so use the recommended CFL inverter.

3.1 Absolute Maximum Ratings

Ta = 25°C

Item	Symbol	Rating	Unit
Lamp voltage	V_S	2000 max.	V rms
Lamp current	I_{FL}	7.0 max.	mA rms
Frequency	f_{FL}	100 max.	kHz

3.2 Electrical Characteristics

Item	Symbol	Conditions	Standard			Unit
			min.	typ.	max.	
Lamp current*	I_{FL}	Ta = 25°C	4.0	5.0	6.0	mA rms
Starting voltage**	V_S	Ta = 0°C	–	–	1000	V rms

* CFL condition : V_{FL} = 390 V rms, f_{FL} = 50 kHz

** With the rise in voltage between the CFL terminals, the glow discharge is generated at the CFL electrodes, and CFL lights as this discharge grows. The starting voltage is the voltage at which the light has become stable and maintainable.

3.3 Brightness

Brightness and the starting voltage of CFL change according to the ambient temperature. This is because the radiation efficiency of the mercury in the CFL lamp varies depending on the vapor pressure. Particularly, the brightness decreases at low temperatures. Brightness is also low immediately after CFL power-on, since the vapor pressure of the mercury is low. Brightness increases gradually with increasing mercury vapor pressure, as the CFL lamp generates heat and thus the lamp wall temperature rises.

Item	Symbol	Conditions	LCD	規 格			単位
				min.	typ.	max.	
Brightness* (At the center of the LCD surface)	Bp	Ta = 25°C 30% to 85%RH 10 min. after CFL power ON	FSTN type (blackand white)	70	100	–	cd / m²
			STN type (blue)	80	100	–	

* CFL inverter : HIU-168 (HARRISON)
CFL driving conditions : I_{FL} = 5.0 mA rms, f_{FL} = 50 kHz
LCD driving conditions : optimum Vopr, f_{FRM} = 71 Hz
LCD display pattern : All ON display (All data = "H")

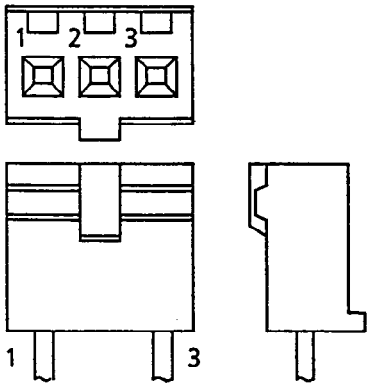
3.4 Service Life

Item	Conditions	Rating	Unit
Service life *	Ta = 25℃ ± 3℃	>12000	h

* Time until the brightness decreases to half of the initial brightness, or time until the CFL is not lit because of the increase in CFL starting voltage.
CFL driving conditions : I_{FL} = 5 mA rms

3.5 Connector for CFL Backlight

Connector for CFL backlight: Socket IL-G-3S-S3C2 (JAE)
Contacts IL-G-C2-SC-10000 (JAE)



No.	Signal	Wire color	Functions
1	V_{FLG}	White	Ground* : 0 V
2	NC	–	NC
3	V_{FL1}	White	CFL backlight drive signal I_{FL} = 5 mA rms, f_{FL} = 50 kHz

* Not connected to the LCD driver ground

Figure 16

3.6 Recommended CFL Inverter

3.6.1 Model name

HIU-168 (HARRISON)

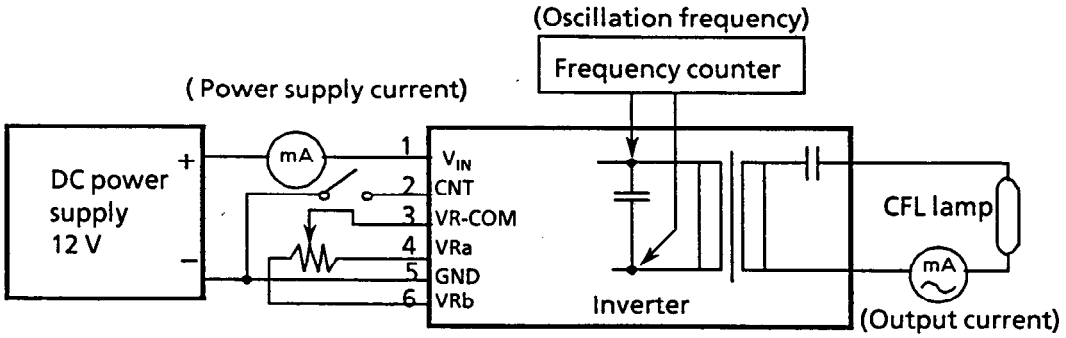
3.6.2 Electrical characteristics

Ta = 25°C ± 3°C

Item	Symbol	Conditions	Standard			Unit
			min.	typ.	max.	
Power supply voltage	V_{IN}		10.8	12.0	13.2	V
Power supply current	I_{IN}	V_{IN} = 12.0 V	–	320	450	mA
Oscillation frequency	f	V_{IN} = 12.0 V Maximum brightness*	40	50	60	kHz
No load output voltage	V_{out}	V_{IN} = 12.0 V Maximum brightness*	1300	1650	–	V 0-p
Output current	I_{out}	V_{IN} = 12.0 V Maximum brightness*	5.0	6.0	7.0	A rms
		V_{IN} = 12.0 V Minimum brightness*	2.3	3.0	–	
Control	CNT	V_{IN} = 10.8 to 13.2 V	– **	– **	– **	–

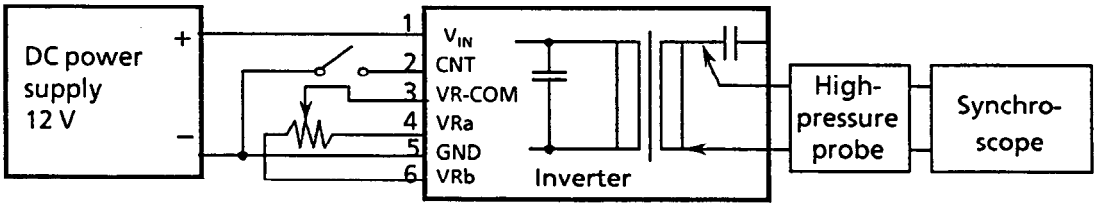
* Brightness is maximum when the resistance between VRa and VR-COM is 0 Ω, and minimum when 10 kΩ.
** On: Low (0.4 V max.)
Off: Open

• Measurement circuit



Item	Measuring instruments
Power supply current	Digital multimeter: FLUKE 8842A or equivalent
Oscillation frequency	Frequency counter: ADVANTEST TR5823H or equivalent
Output current	Thermocouple ammeter: YOKOGAWA TYPE 2016 CLASS 1.0 or equivalent

Figure 16 Measurement Circuit 1



Item	Measuring instruments
No load output voltage	Synchroscope: IWATSU DS-6121A or equivalent High-pressure probe: IWATSU HV-P30 or equivalent

Figure 17 Measurement Circuit 2

3.6.3 Environmental characteristics

Item	Symbol	Conditions	Standard
Operating temperature and humidity	Ta	No freezing or condensation	0°C to + 50°C 90% RH or less
Storage temperature and humidity	Ts	No freezing or condensation	− 20°C to + 60°C, 95% RH or less

3.6.4. Inverter connection diagram (HIU-168)

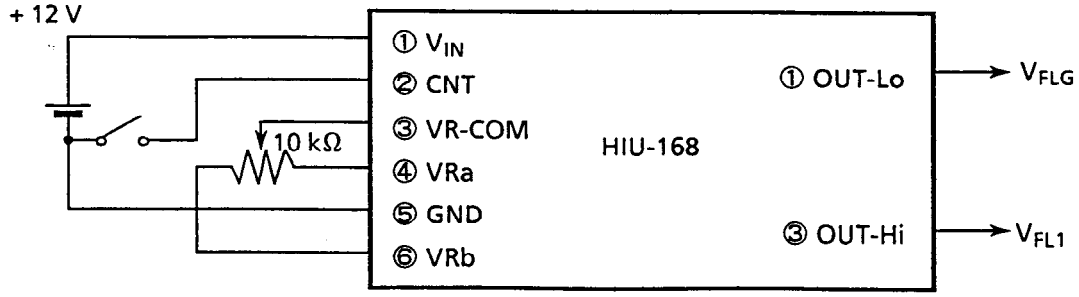


Figure 18 Inverter Connection Diagram

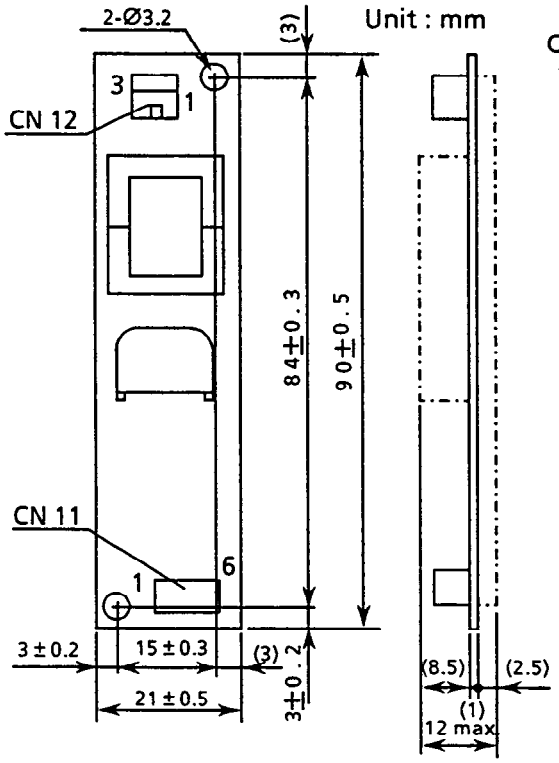
3.6.5 Backlight ON/OFF control

The ON and OFF of the backlight is controlled using CNT pin; the backlight is on when CNT pin is connected to GND and off when CNT pin is open.

3.6.6 Brightness adjustment

Brightness is adjusted using the VRa, VRb and VR-COM pins. Connect a variable resistor of 10 kΩ between VRa and VRb as shown in Fig. 18. Adjust the brightness by changing the resistance.

3.6.7 Dimensions



CN 11 : DF13-6P-1.25H (HIROSE)

Pin No.	Signals	Functions
1	V_{IN}	Power supply voltage: + 12 V
2	CNT	Backlight on/off control
3	VR-COM	Brightness adjustment
4	VRa (10 kΩ)	Brightness adjustment
5	GND	Ground: 0 V
6	VRb (10 kΩ)	Brightness adjustment

Mating connector : DF13-6S-1.25C (HIROSE)

CN 12 : IL-G-3P-S3L2-E (JAE)

Pin No.	Signals	Functions
1	OUT-Lo	Output
2	NC	—
3	OUT-Hi	Output

Figure 19

3.6.8 Precautions in using the inverter

When connecting the inverter to the CFL, the following must be considered to avoid stray capacity effects:

- Do not twist together or tie the CFL connector cables.
- Metal plates and metal foils, if located close to the CFL and its wiring, affect the brightness and the starting voltage of the CFL.
- Connect the CFL connector directly to the inverter output connector. Do not use an extension cable.

4. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal material in your mouth. If the liquid crystal material touches your skin or clothes, wash it off immediately using soap and plenty of water.
- High voltage is present between CFL electrodes. To prevent electric shock, do not touch the wiring while the power is on. Be sure to turn the power off when connecting or disconnecting the connector.

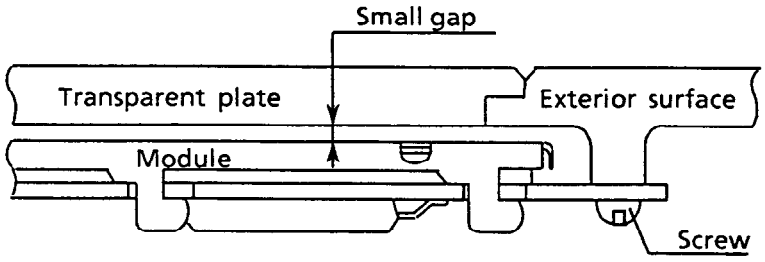
Handling

- Avoid static electricity, as this can damage the CMOS LSI.
- The LCD panel is made of plate glass; do not hit or press against it.
- Do not remove the panel or frame from the module.
- The polarizer on the display is very fragile; handle it very carefully.

Mounting and Design

- Mount the module using the specified installation sections and holes.
- To protect the module from external pressure, put a plate of transparent material such as acrylic or glass over the display surface, frame, and polarizer. Leave a small gap between the transparent plate and the module.

☆Example



- Keep the module dry. Condensation can damage the transparent electrodes.
- If the CFL lamp and its wiring are located close to a metal plate or metal foil, the stray capacity will cause the voltage to fall, which will decrease the brightness and increase the starting voltage. Be careful in designing the casing and the CFL wiring.

Storage

- Store the module in a dark place where the temperature is 25°C ±10°C and the humidity is below 65%RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jar the module or its components.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizer.

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